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EXAMINER	
HENDERSON, ADAM	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,402	MABUCHI ET AL.	
	Examiner	Art Unit	
	Adam L. Henderson	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-24* is/are rejected.

7)☒ Claim(s) *19 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (US Patent 5,698,874). Claims 1 and 14 recite the same essential limitations and therefore any rejection of the device of claim 1 would inherently reject the method disclosed in claim 14. In FIGS. 10A and 10B and lines 47-67 of column 1, Hayashi discloses a solid-state imaging device with pixels that comprise a photodiode, this is inherent in Hayashi's disclosure since a photodiode may be broadly defined as any semiconductor that converts light to electrical energy. Hayashi discloses the use of semiconductor elements in just such a use as a optical transducer. A transistor T_r is disclosed as having a negative gate voltage at the p^+-gate during the period of charge accumulation (see specifically column 1 lines 50-59). Lines 50-59 of column 1 describe incident light generating holes (charge accumulation) and then it states "the p^+-gate is preset at a negative potential." This statement shows that the p^+-gate is set to a negative voltage throughout the entire accumulation period.

3. Claims 4, 5, 20, and 21are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (US Patent 5,892,253). In regards to claims 4 and 20, both of which recite the same essential limitations, Merrill describes a solid-state image pickup device that is composed of a photogate (in the abstract, line 2, this is disclosed as being equivalent to a photodiode in purpose and serves as the photodetector) and a transistor. The voltage applied to the circuit during the charge accumulation period is positive (see column 1 lines 32-57). Specifically lines 51-53 of column one describe how light energy penetrates the substrate 12 of FIG. 1, thus it is equally

definable as a "light receiving surface". FIG. 1 shows this substrate, as broadly recited, as being beside the other components of the circuit and thus inherently beside the electrode.

In regards to claim 5 and 21, both of which recite the same essential limitations, in column 2 lines 5-9 Merrill describes the region under the transistor as having an inverted voltage.

4. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Gaboury et al. (US Patent 5,291,044). Referring to FIG. 1, Gaboury et al. discloses solid-state image pickup device including pixels comprising a photodiode, a detection portion 17 (column2 line 59 and line 66), and a transistor (specifically shown in FIGS. 4 and 5). An overflow path 13 is shown in FIG. 1 and described in column 2 lines 52-67.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US Patent 5,698,874) in view of Merrill (US Patent 5,892,253). Hayashi discloses a solid-state image pickup device as related to claims 1 and 14 above. However, there is no disclosure concerning a channel portion where the voltage is inverted. Merrill discloses the voltage under the transfer gate as being inverted (see column 2 lines 5-16). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Hayashi to include the voltage inverted substrate in order to allow "flow through the inverted surface region under the gate" (column 2 lines 12-13).

7. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US Patent 5,698,874) in view of Burr et al. (5,650,340). Hayashi discloses a solid-state image

pickup device as related to claims 1 and 14 above. However, there is no disclosure concerning. The negative voltage being –0.5V or less. Burr describes a voltage threshold (Vv) between (-) 150 and (+) 150 millivolts within a gate voltage (V_{os}) for the embodiment of the invention (column 9, lines 21-25). Burr further describes that, due to processing variations, the exact dopant concentration (impurity concentration) in the channel region (under the gate) can vary from device to device. Within these variations, a change in threshold voltage (VT) may vary by tens or even hundreds of millivolts (column 9, lines 49-55). With that said, the gate voltage (V_{Gs}) must be capable of having a negative voltage of (-) 0.5 volts or less. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Hayashi to include a negative gate voltage, which is set to (-) 0.5 volts or less. One would have been motivated to combine the image sensor of Hayashi to include the negative gate voltage of (-) 0.5 volts or less of Burr in that a slight variation from device to device (causing significant change in the threshold voltages) is realistic in that there are variations in processing (column 9, lines 49-55).

8. Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,253 to Merrill in view of U.S. Patent No. 4,733,286 to Matsumoto. Merrill describes the solid-state image pickup device as claimed in claim 4 and the solid-state image pickup device driving method as claimed in claim 20, but does not teach the device wherein a positive voltage is set to a power source voltage or more. Matsumoto describes a forward voltage bias applied to a gate electrode (figure 1, item 6) and (column 2, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include a positive voltage on the gate that is set to a power source voltage or

more. One would have been motivated to combine the positive voltage applied to the photogate (PG) (Merrill: figure 1, item 18) to include the forward voltage bias (or source voltage) being applied to the gate electrode of Matsumoto in that an output which is amplified with respect to the light output (photodiode) can now be obtained (Matsumoto: column 2, lines 6-8).

9. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (US Patent 5,892,253) in view of Nakagawa (US Patent 5,862,253).

With regard to claim 7, Merrill claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein an overflow path is formed of an area extended from the portion just below said photodiode to a semiconductor substrate and said area is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51)

which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said region extending from just below the photodiode to the p-type semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

With regard to claim 8, Merrill claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein said overflow path is formed in the area between said photodiode and said detection portion in each pixel is formed of an n-type semiconductor region having an impurity concentration Lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration Lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15- 25) and (Nakagawa: column 17, claim 1). Nakagawa further describes the n-type semiconductor region (or n-type buried Layer 54), which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, Lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51). Note that a photocoupler is

integrally formed with the p-type semiconductor substrate 51 and functions as a current detection means of the current path, therefore comprising that of a detection portion. Since, the p- type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said overflow path is formed in the area between said photodiode: and said detection portion. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region being in the area between the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

With regard to claim 9, Merrill claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein an overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, Lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer

303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, Lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However Nakagawa describes the n-type semiconductor region (or n-type buried Layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type Layer 303. Keep in mind that this area described as "below the photodiode" simultaneously comprises that of the "area between said photodiode and said detection portion," since the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Merrill to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a Low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

10. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaboury (US Patent 5,291,044) in view of Nakagawa (US Patent 5,862,253).

With regard to claim 11, Gaboury discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein an overflow path is formed of an area extended from the portion just below said photodiode to a semiconductor substrate and said area is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration Lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Gaboury to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said region extending from

just below the photodiode to the p-type semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Gaboury to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

With regard to claim 12, Gaboury discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein said overflow path is formed in the area between said photodiode and said detection portion in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15- 25) and (Nakagawa: column 17, claim 1). Nakagawa further describes the n-type semiconductor region (or n-type buried Layer 54), which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, Lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51). Note that a photocoupler is integrally formed with the p-type semiconductor substrate 51 and functions as a current detection means of the current path, therefore comprising that of a detection portion. Since, the p- type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore,

it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Gaboury to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said overflow path is formed in the area between said photodiode: and said detection portion. One would have been motivated to combine the solid-state image pickup device of Gaboury to include the n-type region impurity concentration lower than the p-type region and n-type region being in the area between the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

With regard to claim 13, Gaboury discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein an overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, Lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor

substrate. However Nakagawa describes the n-type semiconductor region (or n-type buried Layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Keep in mind that this area described as "below the photodiode" simultaneously comprises that of the "area between said photodiode and said detection portion," since the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Gaboury to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Gaboury to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US Patent 5,698,874) in view of Isogai et al. (US Patent 5,942,774). Hayashi discloses a solid-state image pickup device as related to claim 14 but does not disclose that charges overflow to the substrate. Isogai et al. disclose in column 16 lines 66-67 the use of the substrate as a location to

send overflow. It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the solid-state image pickup device of Hayashi to include the transmission of overflow to the substrate as taught by Isogai et al. in order to suppress blooming and smear (column 8 lines 60-63).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US Patent 5,698,874) in view of Suzuki (US Patent 6,002,123). Hayashi discloses a solid-state image pickup device as related to claim 14 but does not disclose that charges overflow to the channel of a transistor. Suzuki discloses the excess charge overflowing into the channel of a transistor (column 8 lines 18-21). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Hayashi to include the overflow into the channel of a transistor as taught by Suzuki in order to prevent blooming (column 8 lines 28-38).

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (US Patent 5,892,253) in view of Isogai et al. (US Patent 5,942,774). Hayashi discloses a solid-state image pickup device as related to claim 14 but does not disclose that charges overflow to the substrate. Isogai et al. disclose in column 16 lines 66-67 the use of the substrate as a location to send overflow. It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the solid-state image pickup device of Merrill to include the transmission of overflow to the substrate as taught by Isogai et al. in order to suppress blooming and smear (column 8 lines 60-63).

14. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (US Patent 5,892,253) in view of Suzuki (US Patent 6,002,123). Hayashi discloses a solid-state image pickup device as related to claim 14 but does not disclose that charges overflow to the

channel of a transistor. Suzuki discloses the excess charge overflowing into the channel of a transistor (column 8 lines 18-21). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Merrill to include the overflow into the channel of a transistor as taught by Suzuki in order to prevent blooming (column 8 lines 28-38).

Allowable Subject Matter

15. Claims 19 and 25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments, see pages 8 and 9, filed 4/19/2005, with respect to the rejection(s)of claim(s) 1-2 and 14-15 under Merrill (US Patent 5,892,253) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hayashi (US Patent 5,698,874).

17. Applicant's arguments, see page 10, filed 4/19/2005, with respect to the rejection(s)of claim(s) 10 under Merrill have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gaboury et al. (US Patent 5,291,044).

18. Applicant's argument, see pages 9 and 10, filed 4/19/2005, with respect to amended claims 4 and 20 have been considered but are not considered persuasive. The grounds of rejection remain with the additional explanation that Merrill does disclose that the gate electrode is broadly "beside" Merrill's disclosed light-receiving surface. Where the light-receiving surface

consists of a substrate that allows light energy to penetrate it and thus could be called a "light-receiving surface" (see column 1 lines 51-53 and FIG 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam L. Henderson whose telephone number is 571-272-8619. The examiner can normally be reached on Monday-Friday, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALH
August 15, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER